UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,130	12/30/2003	Alessia Pavan	2110-99-3	3296

996 7590 08/24/2005

GRAYBEAL, JACKSON, HALEY LLP
155 - 108TH AVENUE NE
SUITE 350
BELLEVUE, WA 98004-5901

EXAMINER	
FARAHANI, DANA	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,130	PAVAN ET AL.	
	Examiner	Art Unit	
	Dana Farahani	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 15-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-14 and 27-30* is/are allowed.

6)☒ Claim(s) *1-6 and 15-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicants' election with traverse of claims 1-6 and 15-26 in the reply filed on 8/4/05 is acknowledged. The traversal is on the grounds that the search for all of the claims is not a serious burden, and therefore the examiner has to examine all the claims This is not found persuasive because as set forth in the restriction requirement mailed on 7/12/04, the memory cell structure in the device claims can be made with a method other than the method specified in the method claims, and therefore, the method claims require a separate search.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Regarding claim 5, the phrase "for example" renders the claim indefinite because it is unclear whether the limitation following the phrase is part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable Nakajima et al., hereinafter Nakajima (US Patent 5,614,748) in view of Catabay et al., hereinafter Catabay (US Patent 6,800,940).

Regarding claims 1, 4, and 6, Nakajima discloses in figure 1, a non-volatile memory comprising:

a floating gate transistor including a source region 24b and a drain region 24a, a gate region projecting from the substrate and comprised between said source and drain regions, said gate region having a predetermined length and width and comprising a first floating gate region 8 and a control gate region 12, characterized in that said floating gate region is insulated laterally, along the width direction, by a dielectric layer 14 with a dielectric constant value.

Nakajima does not disclose the low dielectric constant value is between 1 and 3.9 (low dielectric), and the layer is formed by an oxide layer, hydrated with alkylic groups.

Catabay discloses in figure 4, and column 6, lines 23-37, a carbon doped silicon layer 30 in the integrated circuit structure shown. Catabay further discloses this kind of layer is void free and have a dielectric constant of less than 3 (see column 4, lines 35-40 and 52-55), further disclosing low dielectric constant values reduces horizontal capacitance between conductive lines (see column 2, lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use carbon doped oxide layer in the structure of Nakajima to benefit from the advantageous properties of the layer such as reduced capacitance between the gate electrodes. Note that using alkylic groups to dope the oxide layer is a method of doping the oxide layer.

Regarding claim 2, the floating gate regions are covered by a dielectric layer 30a before being insulated from each other through said dielectric layer with low dielectric constant value (see figure 3D).

Regarding claim 3, the dielectric layer with low dielectric constant value is bounded between said floating gate regions, as can clearly be seen in figure 1.

6. Claims 15-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima in view of Catabay and further in view of Lee et al., hereinafter Lee (US Patent 6,717,846).

Regarding claims 15, 16, 18, 21, 24, and 25, Nakajima in view of Catabay substantially discloses the limitations in the claims, as discussed above, except for expressly stating the cells are organized in a matrix form.

Lee discloses memory cells are arranged in rows and column (figure 2a) to make a memory array. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the memory cell of the Nakajima reference in a matrix form, since memory cells are normally arranged in a matrix pattern to make them usable in various applications.

Regarding claims 17 and 23, the memory cell of Nakajima has an ONO dielectric layer 10 having a greater dielectric constant than the insulating regions formed on the floating gate regions.

Regarding claims 19, 20, 22, and 26, note that the gates of the transistors in the Lee reference are connected to each other and the cells are flash memory cells. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the memory cell of the structure of Nakajima in view of Catabay in a storage memory matrix form

with the gates of the cells connected, to take advantage of the benefits the cell offers, such as low leakage current (see Nakajima, column 1, lines 60-67).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER